

**IN THE SPECIFICATION:**

Please replace the paragraph at page 42, lines 10-18 with the following amended paragraph:

The driver circuit is composed of logic circuits such as a buffer circuit, the shift ~~resister~~ register circuits or the like, as well as a sampling circuit formed of an analog switch, or the like. In Fig. 8B, the TFTs for forming these circuits are illustrated to have a single-gate structure in which only one gate electrode is provided between a pair of source and drain regions. However, a multigate structure in which a plurality of gate electrodes are provided between a pair of source and drain regions may also be used.

Please replace the paragraph at page 60, lines 4-9 with the following amended paragraph:

The image signal driver circuit 606 comprises a shift ~~resister~~ register circuit 501a, a level shifter circuit 502a, a buffer circuit 503a, and a sampling circuit 504. In addition, the scanning signal driver circuits (A) and (B) 185 comprises a shift ~~resister~~ register circuit 501b, a level shifter circuit 502b, and a buffer circuit 503b.

Please replace the paragraph at page 60, lines 10-22 with the following amended paragraph:

The driving voltages of the shift ~~resister~~ register circuits 501a and 501b are between 5 and 16V (typically 10V). A TFT of a CMOS circuit for forming this circuit is formed of the first p-channel TFT 200 and the first n-channel TFT 201 of Fig. 8B, or the

TFT may be formed of the first p-channel TFT 280 and the first n-channel TFT 281 shown in Fig. 12A. In addition, since the driving voltage of the level shifter circuits 502a and 502b and the buffer circuits 503a and 503b become as high as 14 to 16V, it is preferable that the TFT structure be formed into a multi-gate structure as shown in Fig. 12A. Forming the TFT into a multi-gate structure is effective in raising voltage-resistance and improving the reliability of the circuits.